WHAT IS CLAIMED IS:

1. A conditional clock buffer circuit having a clock output and coupled to receive a clock input and a condition signal, the conditional clock buffer circuit comprising:

a first circuit coupled to receive the clock input, the first circuit configured to generate a first state on the clock output responsive to a first phase of the clock input; and

a second circuit coupled to receive the clock input and the condition signal, wherein the second circuit is configured to conditionally generate a second state on the clock output responsive to the condition signal during a first portion of a second phase of the clock input.

2. The conditional clock buffer circuit as recited in claim 1 further comprising a latch circuit coupled to the first circuit and coupled to the clock output, wherein the latch circuit is configured to hold the clock output during a remaining portion of the second phase.

3. The conditional clock buffer circuit as recited in claim 1 wherein the first portion of the second phase is about 1/4 of the second phase.

4. The conditional clock buffer circuit as recited in claim 1 wherein the first portion of the second phase is about 2 gate delays.

5. The conditional clock buffer circuit as recited in claim 1 wherein the second circuit comprises a first transistor, a second transistor, and a third transistor connected in series, wherein a first control node of the first transistor is coupled to receive the clock input, and wherein a second control node of the second transistor is coupled to receive the

condition signal, and wherein a third control node of the third transistor is coupled to receive an inverse of the clock input with a delay.

6. The conditional clock buffer circuit as recited in claim 5 wherein the inverse of the clock input is generated by a logic gate coupled to receive the clock input and having an output coupled to the third control node.

7. The conditional clock buffer circuit as recited in claim 6 wherein the logic gate is sized to generate the delay of about 1/4 of the second phase.

8. The conditional clock buffer circuit as recited in claim 6 wherein the logic gate is sized to generate the delay of about 2 gate delays.

9. The conditional clock buffer circuit as recited in claim 6 wherein the logic gate is an inverter.

10. The conditional clock buffer circuit as recited in claim 5 wherein the second circuit further comprises a fourth transistor coupled to a node of the second transistor and having a fourth control node coupled to the condition signal, the fourth transistor charging the node in response to the condition signal indicating that the second state is not to be generated on the clock output.

11. A clock tree comprising:

one or more levels of buffering coupled to receive an input clock and output a buffered clock; and

one or more conditional clock buffer circuits coupled to receive the buffered clock and a condition signal, each conditional clock buffer circuit having a clock

output and including:

a first circuit coupled to receive the buffered clock, the first circuit configured to generate a first state on the clock output responsive to a first phase of the buffered clock; and

a second circuit coupled to receive the buffered clock and the condition signal, wherein the second circuit is configured to conditionally generate a second state on the clock output responsive to the condition signal during a first portion of a second phase of the buffered clock.

12. The clock tree as recited in claim 11 wherein the conditional clock buffer circuit further comprises a latch circuit coupled to the first circuit and coupled to the clock output, wherein the latch circuit is configured to hold the clock output during a remaining portion of the second phase.

13. The clock tree as recited in claim 11 wherein the first portion of the second phase is about 1/4 of the second phase.

14. The clock tree as recited in claim 11 wherein the first portion of the second phase is about 2 gate delays.

15. The clock tree as recited in claim 11 wherein the second circuit comprises a first transistor, a second transistor, and a third transistor connected in series, wherein a first control node of the first transistor is coupled to receive the buffered clock, and wherein a second control node of the second transistor is coupled to receive the condition signal, and wherein a third control node of the third transistor is coupled to receive an inverse of the buffered clock with a delay.

16. The clock tree as recited in claim 15 wherein the inverse of the buffered clock is generated by a logic gate coupled to receive the buffered clock and having an output coupled to the third control node.

17. The clock tree as recited in claim 15 wherein the delay defines the first portion of the first phase.

18. The clock tree as recited in claim 15 wherein the second circuit further comprises a fourth transistor coupled to a node of the second transistor and having a fourth control node coupled to the condition signal, the fourth transistor charging the node in response to the condition signal indicating that the second state is not to be generated on the clock output.

19. A computer accessible medium comprising one or more data structures representing:

a first circuit coupled to receive a clock input, the first circuit configured to generate a first state on a clock output responsive to a first phase of the clock input; and

a second circuit coupled to receive the clock input and a condition signal, wherein the second circuit is configured to conditionally generate a second state on the clock output responsive to the condition signal during a first portion of a second phase of the clock input.

20. The computer accessible medium as recited in claim 20 wherein the one or more data structures further represent a latch circuit coupled to the first circuit and coupled to the clock output, wherein the latch circuit is configured to hold the clock output during a remaining portion of the second phase.